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# A Low Dark Current Stacked CMOS-APS for Charged Particle Imaging

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**Abstract**

A stacked CMOS-active pixel sensor (APS) with a newly devised pixel structure for charged particle detection has been developed. A twin well pixel with a p-MOS readout transistor achieves low leakage current caused by a hot carrier effect at low temperature as low as $5\times10^{-8}$ V/s at the pixel electrode. The total read noise floor of 0.1mVrms was obtained by non-destructive readout CDS with the CDS interval of 21 seconds.

## Introduction

Photo-plate or florescent screen with maicrochannel plate has been used for two dimensional detector for mass spectrograph and ion micrograph[1]. Matsumoto *et al.* demonstrated that spatial resolution, linearity and dynamic range of ion micrograph and mass spectrograph were extremely improved by using a Stacked AMI (Amplified MOS Imager) comparing with the conventional system [2].

In addition to the superior performance characteristics, a use of the stacked CMOS-APS provides several advantages, including low voltage operation, low power consumption, long lifetime, stable detectability against mass number and robustness against environment [2, 3].

However, further improvements of noise performance is demanded to obtain an image with higher signal-to-noise ratio.

In this paper, a stacked CMOS-APS with a newly devised pixel structure is presented. The new pixel achieves much lower leakage current and flicker noise than the conventional n-MOS pixel, which permits longer integration time, thereby yielding higher signal-to-noise ratio.

## Stacked CMOS-APS for charged particle detection

Fig. 1 shows a schematic configuration of a conventional n-MOS stacked pixel for charged particle detection. The pixel consists of a readout transistor $M_{RD}$, a select transistor $M_{SEL}$, a reset transistor $M_{RS}$ and a top metal electrode to which signal ions are irradiated directly. The top electrode is connected to the gate electrode of $M_{RD}$ and a source electrode of $M_{RS}$. At the beginning of charge detection period, the top electrode is reset to the reset voltage $V_{RS}$ by turning $M_{RS}$ on. Then signal ions are irradiated onto the top electrode. Charged signal ion with acceleration energy of several keV, generates multiple secondary electrons which are swept away through an external anode electrode. Thus charge of the implanted ions and the positive charge corresponding to the secondary electrons accumulated on a storage capacitor increase the potential of the top electrode. The amount of the accumulated charge can be estimated by reading out the increase of the top electrode potential through source follower circuit with its load being not shown in the figure.

With a stacked CMOS-APS for charged particle detection, long signal integration time is required to obtain a highly accurate two-dimensional ion image since irradiated ion density is very low. The integration time often exceeds one hour in actual usage. Thus the imager is commonly operated at low temperatures to reduce dark current generation. Its read noise floor is dominated by the kTC noise associated with the reset operation and the thermal noise of $M_{RD}$.

Non-destructive readout - correlated double sampling (NDRO-CDS) was introduced to reduce the read noise [4]. In this operation, two images are read out nondestructively, one just after the reset and the other after the integration, and then subtracted, so that both kTC noise and fixed pattern noise are suppressed. As a result, read noise was reduced to $13e^-$ with the NDRO-CDS interval of about 20 sec. The reset noise suppression capability of APS's is one of advantages over stacked CCD imagers. A stacked CCD imager suffers from the kTC noise, due to incomplete charge transfer from the stacked electrode to the CCD channel. In addition, the non-destructive readout capability of APS's can be utilized for real-time monitoring of the charge accumulation during the signal integration.

There are two significant problems with a pixel of the conventional stacked CMOS-APS. One is the dark current due to a hot carrier effect at low temperatures. The other one is the flicker noise of a readout transistor. Because of the long integration period, flicker noise degrades the signal fidelity even with NDRO-CDS operation.

## Dark Current Analysis of the Conventional N-MOS Pixel at Low Temperatures

Fig.2 shows a measurement result of temperature dependence of the dark current in a conventional pixel which consists of n-MOS transistors located in a common p-well [5]. The temperature dependence becomes weak at temperatures below -60°C, while activation energy of 0.5eV is extracted in higher temperature region, which suggests the origin of the dark current is the thermal generation current.

The dark current at such low temperatures increases exponentially with the drain voltage of $M_{RD}$. Fig.3 shows the drain voltage dependence of dark current of the n-MOS active pixel at the temperature of 100K. The pixel test structures used were fabricated in 0.8μm CMOS process. The vertical axis represents the voltage change at the pixel electrode per second. Since the dark currents increase with reduced gate length of the readout transistor, it is considered that a hot carrier effect is involved in the dark current generation. Especially under low temperature such as liquid nitrogen temperature, the hot carrier effect may be more significant than at room temperature. Since the gate of the readout transistor is biased at an intermediate voltage during the source follower operation, the readout transistor tends to be exposed by the impact of hot carriers.

With these results, we assumed two origins of the leakage current caused by hot carrier effect. One is a gate current caused by carrier injection at the readout transistor $M_{RD}$. The other is the photon assisted leakage, where photons generated by hot carriers at the channel region of $M_{RD}$ generate electron-hole pairs, which yield dark current.

## Design and Characterization

Assuming the leakage models mentioned above, we have developed an imager with a new pixel structure which achieves lower leakage current at low operation temperatures. A schematic cross sectional view and a circuit configuration of the pixel is shown in Fig. 4a and 4b, respectively. The imager is fabricated in 0.8 μm twin-well CMOS process on a p-epitaxial wafer. The pixel consists of an n-MOS reset transistor, p-MOS readout and select transistors. For the ion detection applications, the top electrode should be initialized at a low voltage to extend dynamic range, since accumulated signal charge raises the top electrode voltage. Thus n-MOS reset and p-MOS readout configuration is preferable.

Due to the p-MOS readout transistor, the hot carrier effect can also be suppressed because of lower mobility of holes than that of electrons. In addition to the smaller hot carrier generation, an $n^+$/p-well/p-epi junction avoids carrier diffusion from the bulk into the $n^+$ source junction of $M_{RS}$. The photo-generated carriers are then swept away from well contacts. Thus, the dark current caused by the photon is also suppressed. In addition, flicker noise power of p-MOSFET is commonly smaller than that of n-MOSFET. As a result, low dark current at low temperature and low flicker noise are expected with this new pixel structure.

Fig. 5 shows the developed charged particle detection imager. Pixel size is 20μm × 20μm and the number of effective pixels is 600 × 576, yielding the size of image area is 12mm × 11.52mm. Because of the stacked structure, high fill factor of 88% has been achieved, so that highly sensitive ion detection is possible. Read noise of the imager is measured to be 0.1mVrms referred the top electrode voltage with NDRO-CDS where the CDS interval of 21 seconds and 20kHz pixel rate are used. Dynamic range of the imager exceeds 80dB. With a design value of pixel capacitance of 14fF, equivalent noise electron number is estimated to be $9e^-$.

The relationship between the dark signal rate and the drain voltage of $M_{RD}$ is shown in Fig. 6. The dark current has been significantly reduced with the new pixel. The dark signal as low as $5\times10^{-8}$ V/s at the pixel electrode realizes very long signal integration period. For example, when integration time is 1 hour, dark charge is estimated to be $16e^-$ per pixel.

A reproduced image of $Al^+$ ion density distribution obtained with the imager is shown in Fig. 7. The NDRO capability of the imager is utilized to monitor the charge accumulating condition during the signal integration period.

## Conclusion

We have developed a low dark current stacked CMOS APS for charged particle detection in which a newly devised pixel is implemented. A use of a p-MOS FET for a readout transistor reduces a hot carrier effect, thereby the dark current in low temperature region was extremely decreased. It also improved read noise performance because of its lower flicker noise than n-MOSFETs'. The low dark current, low read out noise and high fill factor of the imager permit accurate charged particle image capturing for applications such as ion and electron imaging.

## References


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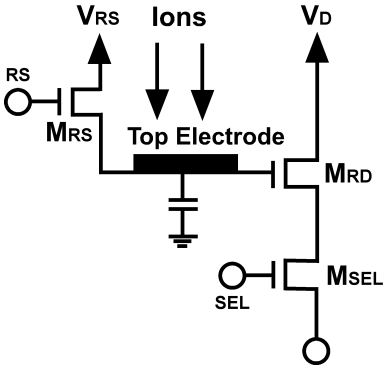


Fig.1. Schematic configuration of a stacked type pixel for charged particle imaging. Secondary electrons generated by the incident ions are drained to an external anode electrode, and both charges of incident ions and drained secondary electrons are accumulated at the top electrode.

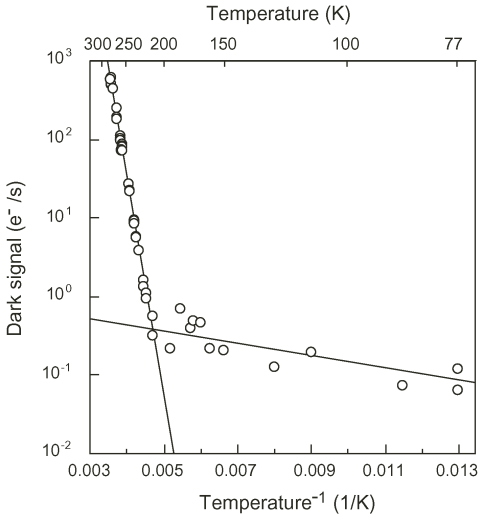


Fig.2. Temperature dependence of dark signal of the conventional stacked CMOS-APS with n-MOS active pixels.

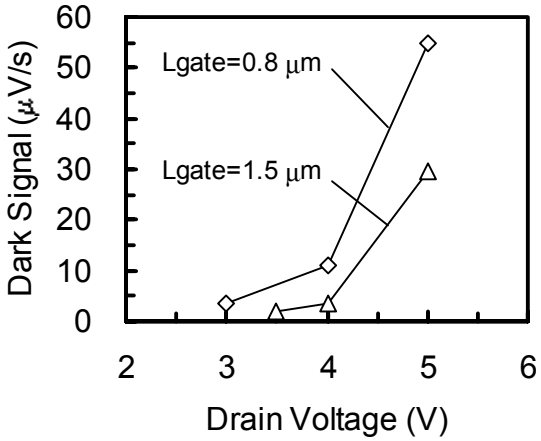


Fig. 3. Drain voltage dependence of the dark signal of the conventional n-MOS pixel at T=100K. Except for the gate length of the readout transistor $M_{RD}$, pixel layouts are identical.

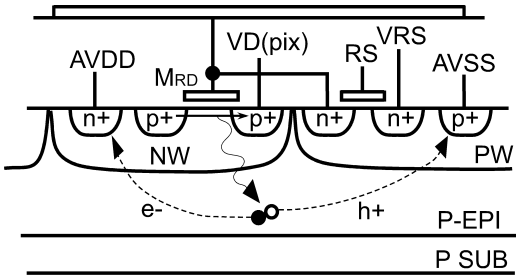


Fig. 4a. A cross sectional view of a proposed pixel structure. The readout and reset transistors are formed by p-MOS and n-MOS transistor, respectively.

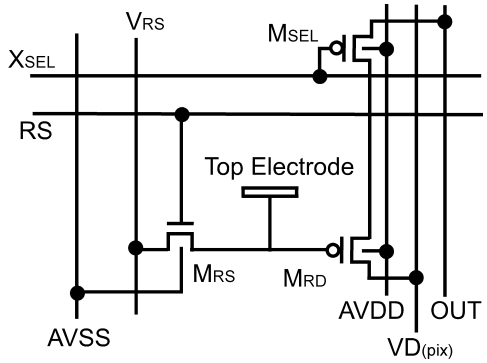


Fig. 4b. Circuit configuration of the pixel. Transistor dimension of $M_{RD}$ is W/L=1.8μm/1.1μm.

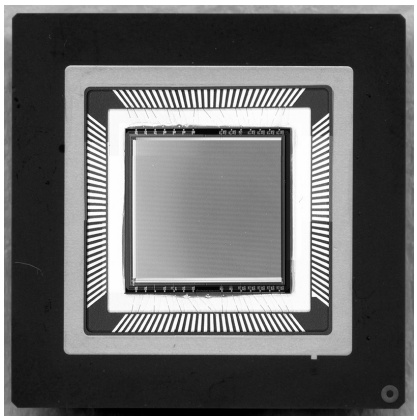

Fig. 5. Developed charged particle imager, having 600×576 effective pixels with 20μm pixel pitch.

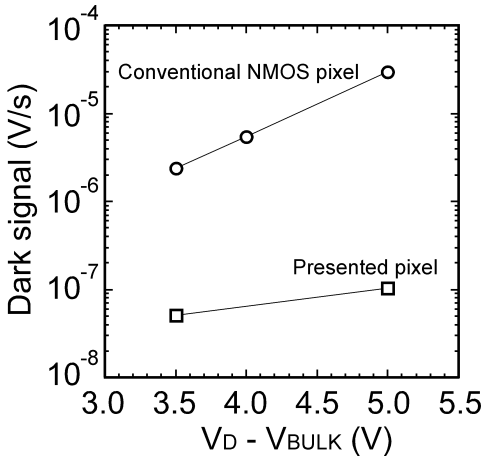


Fig. 6. Comparison of dark currents at T=100K between the conventional n-MOS type pixel and the presented pixel. Both pixels have same transistor size and layout except for polarity of $M_{RD}$ and $M_{SEL}$.

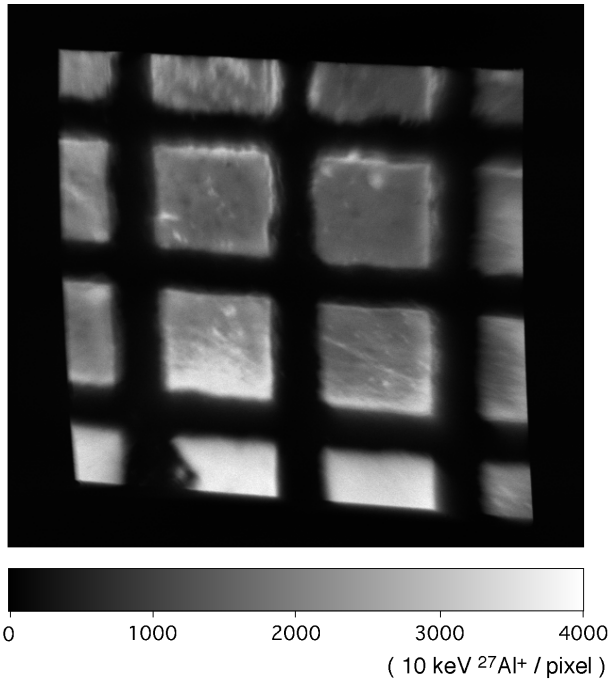


Fig. 7. A reproduce image obtained by the imager. The sample is an Al target on which Cu grids are located. The bright areas are the aluminum regions of the sample.